ABSTRACT OF THE DISCLOSURE

A prescaler generally comprising a first circuit, a multiplexer, and a second circuit. The first circuit may be configured to present a plurality of control signals in response to a first clock signal having a first frequency. The multiplexer may be configured to multiplex a plurality of data signals in response to the control signals to present a second clock signal having a second frequency that is a non-integer fraction of the first frequency. The second circuit may be configured to present the data signals in response to the second clock signal.